CLAIMS

1. (Original) A power amplifier circuit comprising:

a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal;

a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal;

a second amplifier subsection configured to receive the delayed input signal, and in response, provide a first delayed output signal;

an impedance inverter circuit configured to provide an impedance inversion and introduce a second delay to the first output signal, thereby creating a second delayed output signal;

means for combining the first and second delayed output signals, thereby creating an amplified output signal; and

a level control circuit configured to provide a first output level control signal that causes the first amplifier subsection operate in a saturated mode when the first amplifier is enabled, and a second output level control signal that causes the second amplifier subsection to operate in a saturated mode when the second amplifier subsection is enabled.

2. (Original) The power amplifier of Claim 1, further comprising bias control circuitry configured to independently enable and disable the first and second amplifier subsections.

3. (Original) The power amplifier of Claim 2, wherein the bias control circuitry comprises a bias control circuit configured to generate a first bias voltage and a second bias voltage in response to an analog level control signal, wherein the first bias voltage is applied to the first amplifier subsection and the second bias voltage is applied to the second amplifier subsection.

4. (Original) The power amplifier of Claim 2, wherein the bias control circuit comprises:

means for activating the first bias voltage and deactivating the second bias voltage when the analog level control signal identifies a low power mode; and

means for activating both the first and second bias voltages when the analog level control signal identifies a high power mode.

5. (Original) The power amplifier of Claim 1, wherein the first output level control signal and the second output level control signal are ramp signals.

6. (Original) The power amplifier of Claim 1, wherein the means for combining comprise an output terminal configured to receive the first and second delayed output signals, wherein an output signal is provided on the output terminal.

7. (Original) The power amplifier of Claim 1, wherein the first amplifier subsection comprises a first transistor, and the level control circuit comprises a first control transistor coupled between a collector of the first transistor and a voltage supply terminal.

8. (Original) The power amplifier of Claim 7, further comprising an inductor coupled between the collector of the first transistor and the first control transistor.

9. (Original) The power amplifier of Claim 7, wherein the second amplifier subsection comprises a second transistor, and the level control circuit comprises a second control transistor coupled between a collector of the second transistor and the voltage supply terminal.

10. (Original) The power amplifier of Claim 9, further comprising:

an inductor coupled between the collector of the first transistor and the first control transistor; and

an inductor coupled between the collector of the second transistor and the second control transistor.

11. (Original) The power amplifier of Claim 1, wherein the first delay circuit comprises an inductor and one or more capacitors.

12. (Original) The power amplifier of Claim 11, wherein the impedance inverter circuit comprises an inductor and one or more capacitors.

13. (Original) The power amplifier of Claim 1, wherein the first amplifier subsection comprises at least one heterojunction bipolar transistor, and wherein the second amplifier subsection comprises at least one heterojunction bipolar transistor.

14. (Original) The power amplifier of Claim 1, wherein the first delay is equal to the second delay.

15. (Previously Presented) A method of amplifying an input signal; comprising:

providing the input signal to a first amplifier subsection;

applying a first bias voltage to a base of the first amplifier subsection to enable the first amplifier;

applying a first output level control signal to a collector of the first amplifier subsection to cause the first amplifier subsection to operate in saturated mode when the first amplifier subsection is enabled, such that the first amplifier subsection provides a first output signal in response to the input signal;

introducing a first delay to the input signal, thereby creating a delayed input signal;

providing the delayed input signal to a second amplifier subsection;

enabling the second amplifier subsection to operate in a saturated mode, wherein the second amplifier subsection provides a first delayed output signal in response to the delayed input signal;

introducing a second delay to the first output signal, thereby creating a second delayed output signal; and

combining the first and second delayed output signals, thereby creating an amplified output signal.

16. (Original) The method of Claim 15, further comprising selecting the first delay to be equal to the second delay, such that the first and second delayed output signals are substantially in phase.

17. (Original) The method of Claim 15, further comprising disabling the second amplifier subsection in a low power mode.

18. (Canceled)

19. (Currently Amended) The method of Claim 15, wherein the first output level control signal is a ramp signal.

20. (Original) The method of Claim 17, wherein the step of enabling the second amplifier subsection to operate in a saturated mode comprises:

applying a second bias voltage to a base of the second amplifier subsection; and

applying a second output level control signal to a collector of the second amplifier subsection.

21. (Original) The method of Claim 20, wherein the second output level control signal is a ramp signal.